FIG. 1

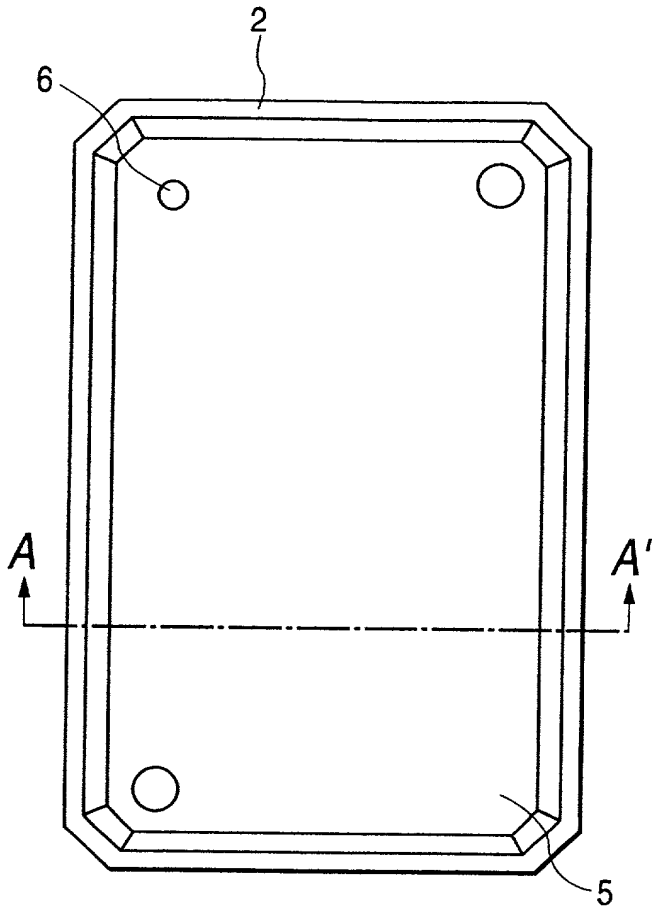


FIG. 3

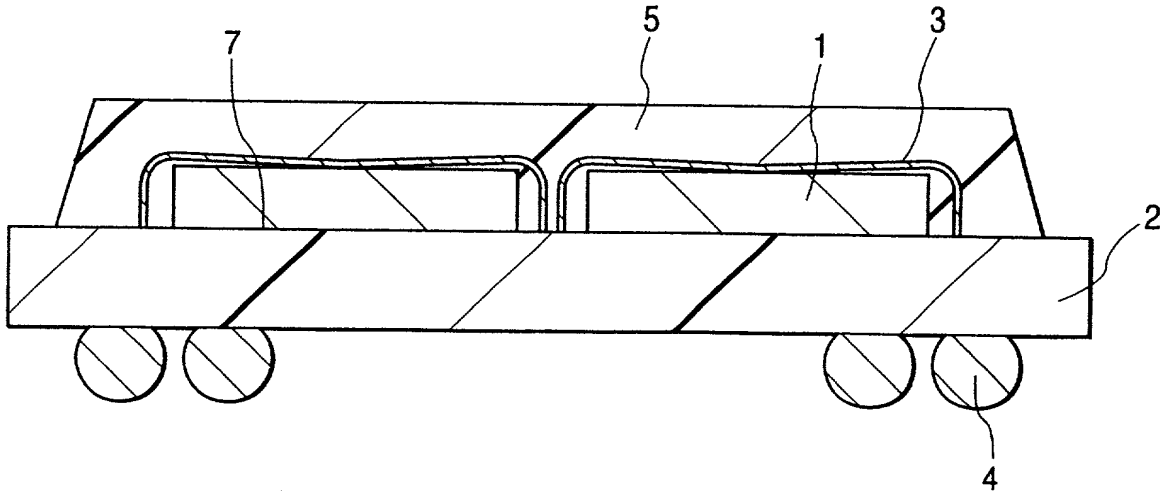


FIG. 2(c)

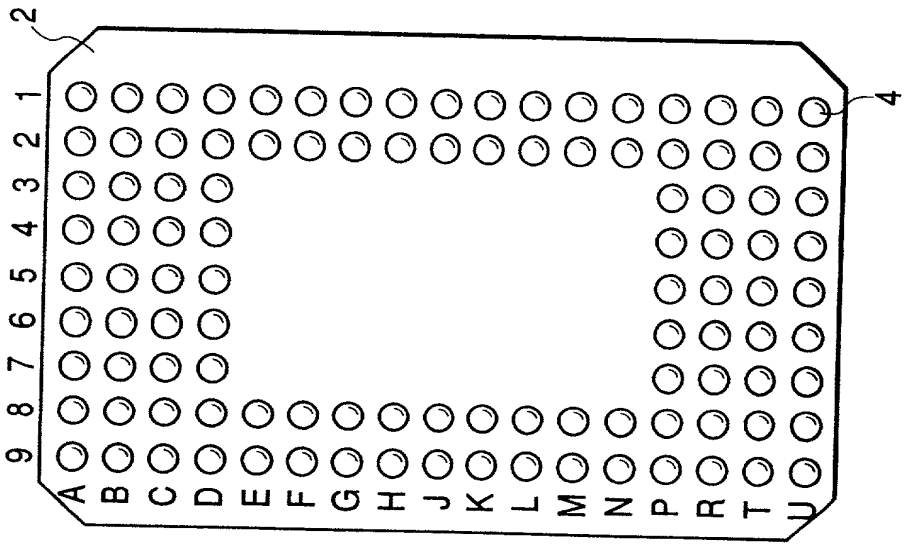


FIG. 2(b)

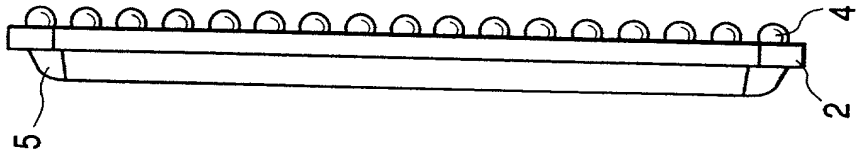


FIG. 2(a)

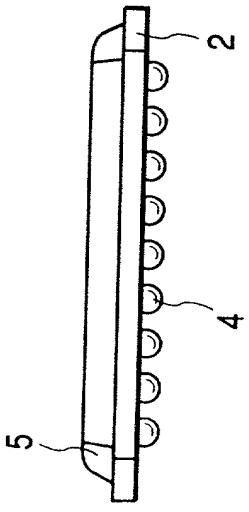


FIG. 4

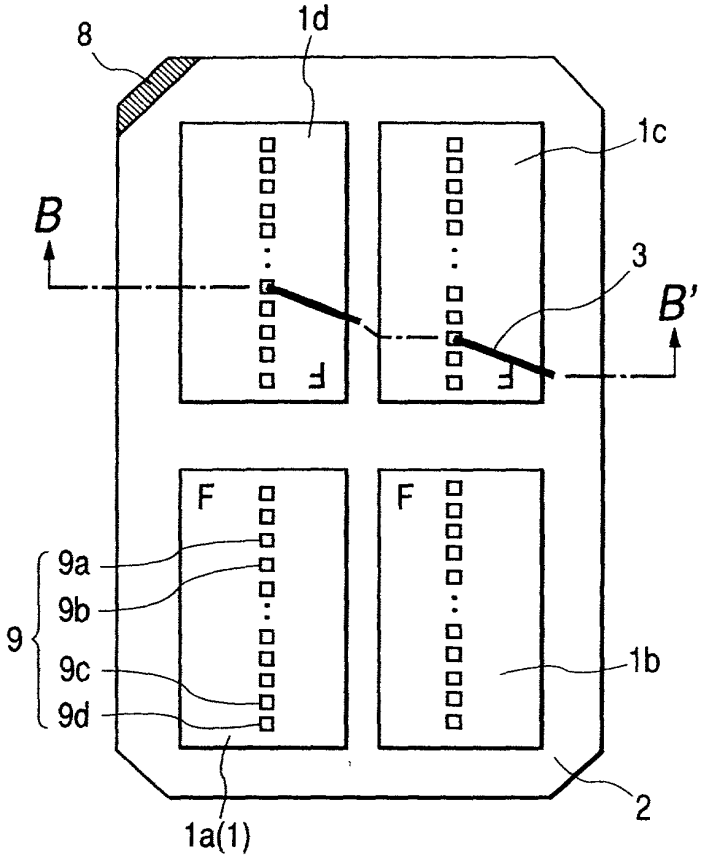

8
1d
1c
B
B'
3
F
F
F
F
9a
9b
9
9c
9d
1b
2
1a(1)

FIG. 5

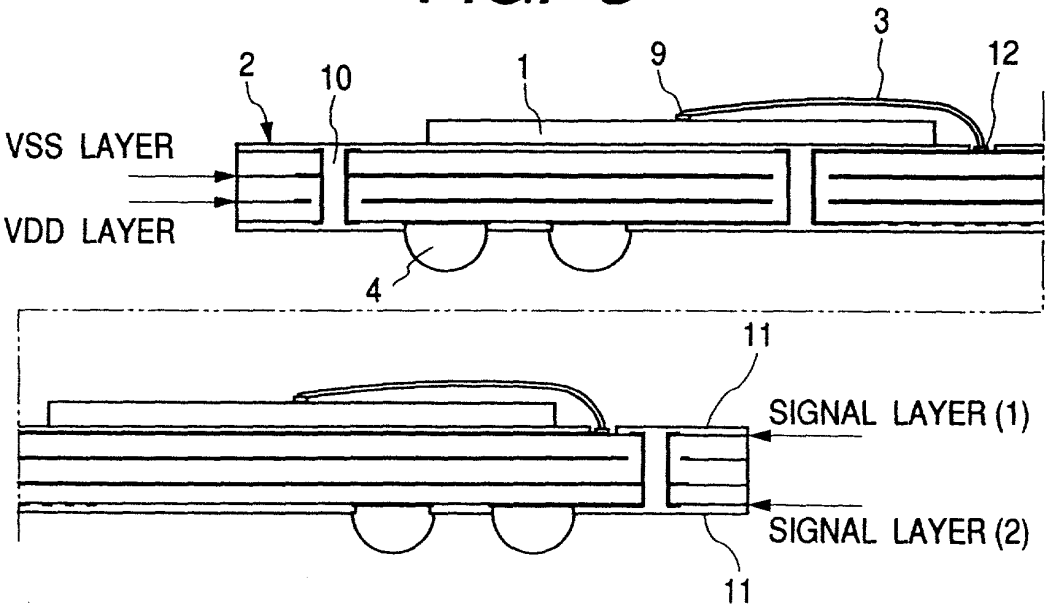

2
10
1
9
3
12
VSS LAYER
VDD LAYER
4
11
SIGNAL LAYER (1)
SIGNAL LAYER (2)
11

FIG. 6

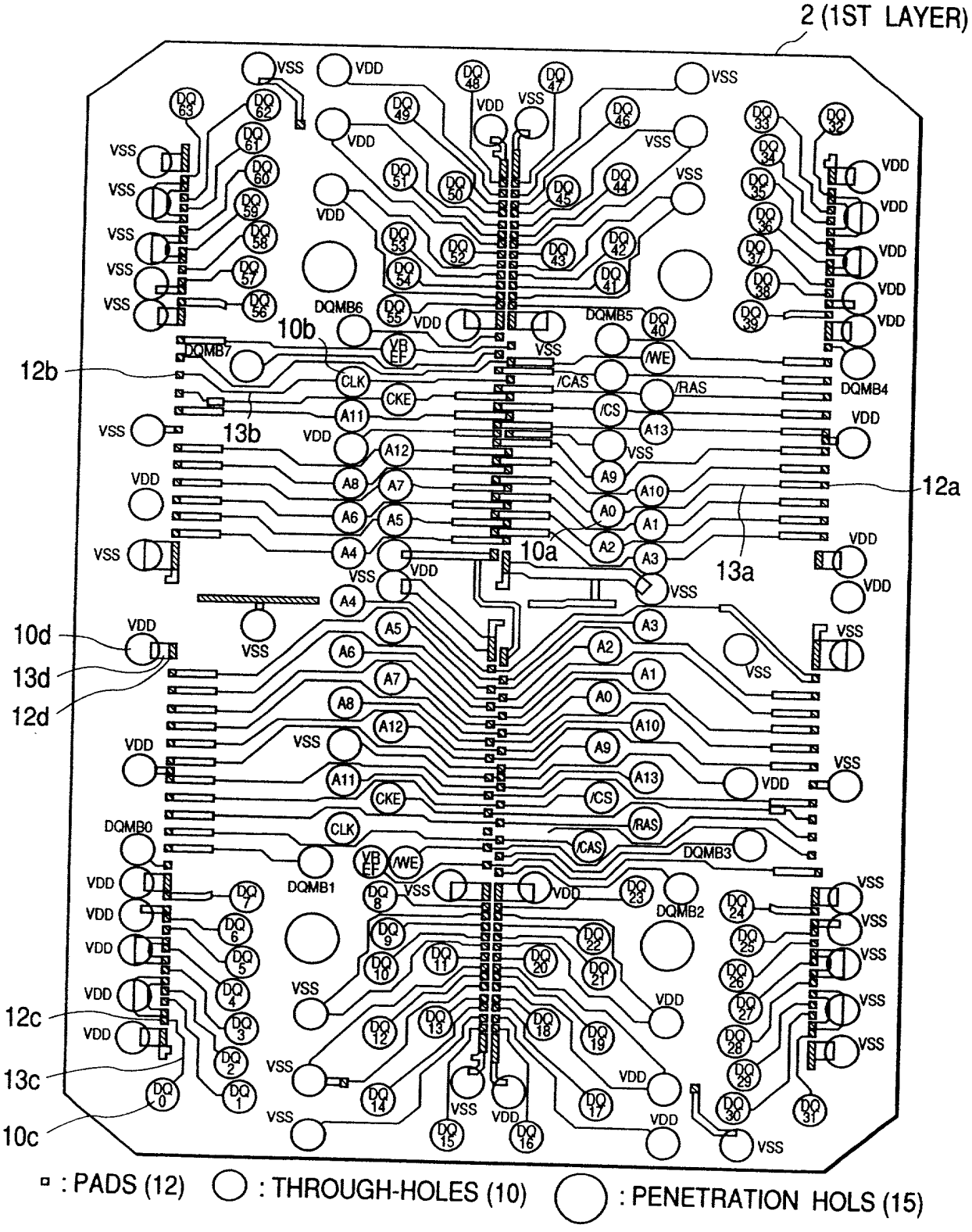

2 (1ST LAYER)
12b
13b
10b
12a
13a
10a
10d
13d
12d
12c
13c
10c
: PADS (12)
: THROUGH-HOLES (10)
: PENETRATION HOLS (15)

FIG. 7

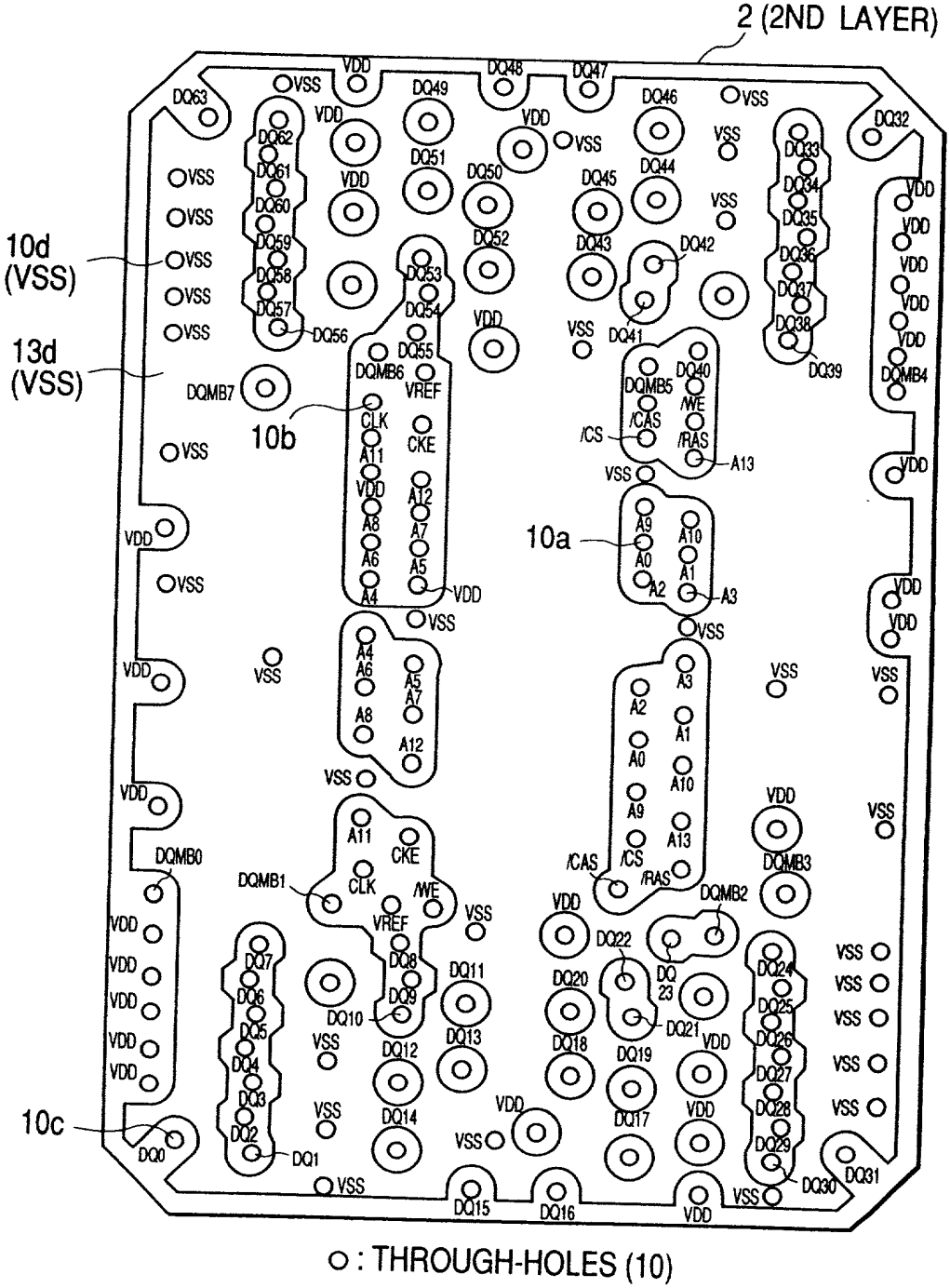


FIG. 8

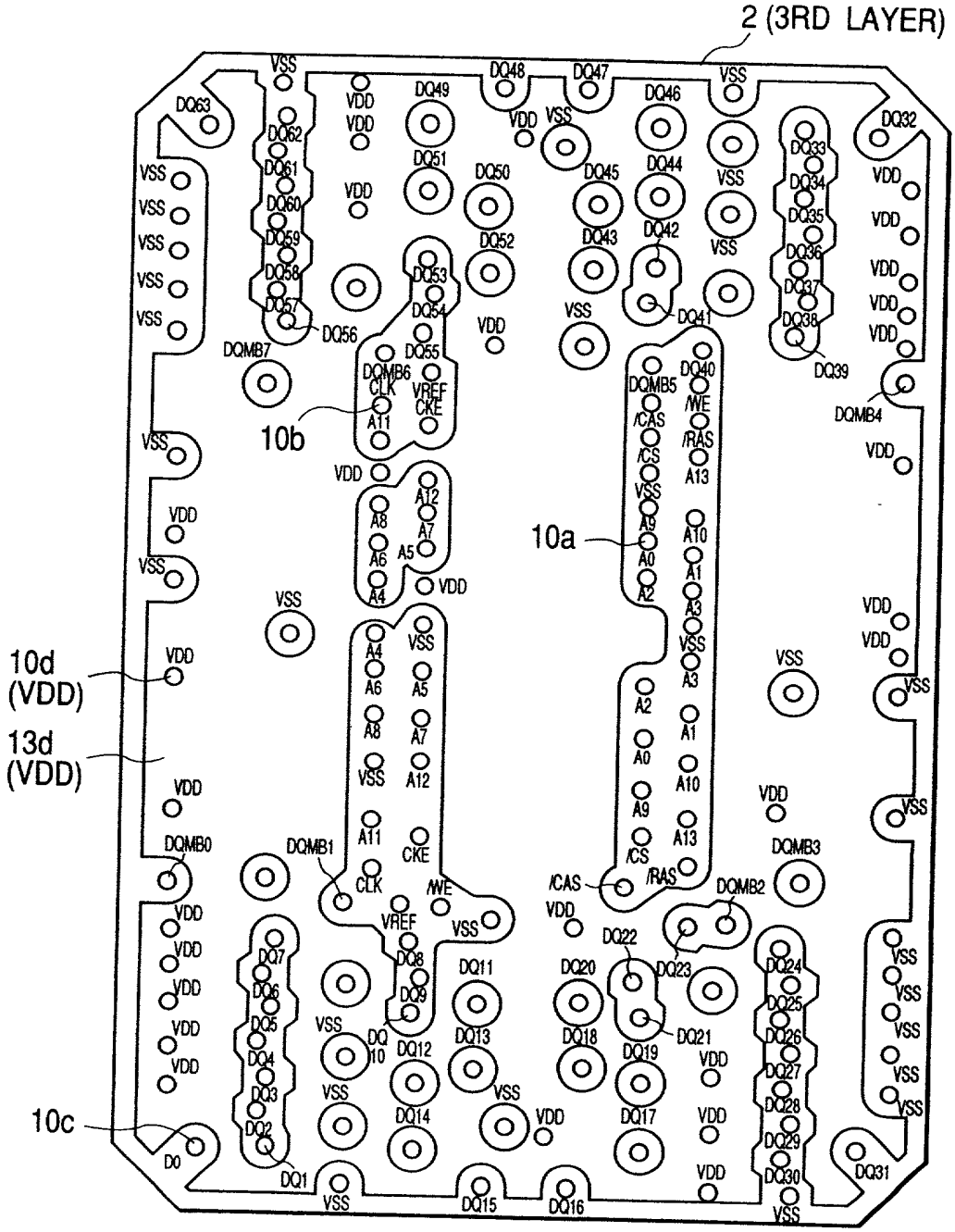


FIG. 9

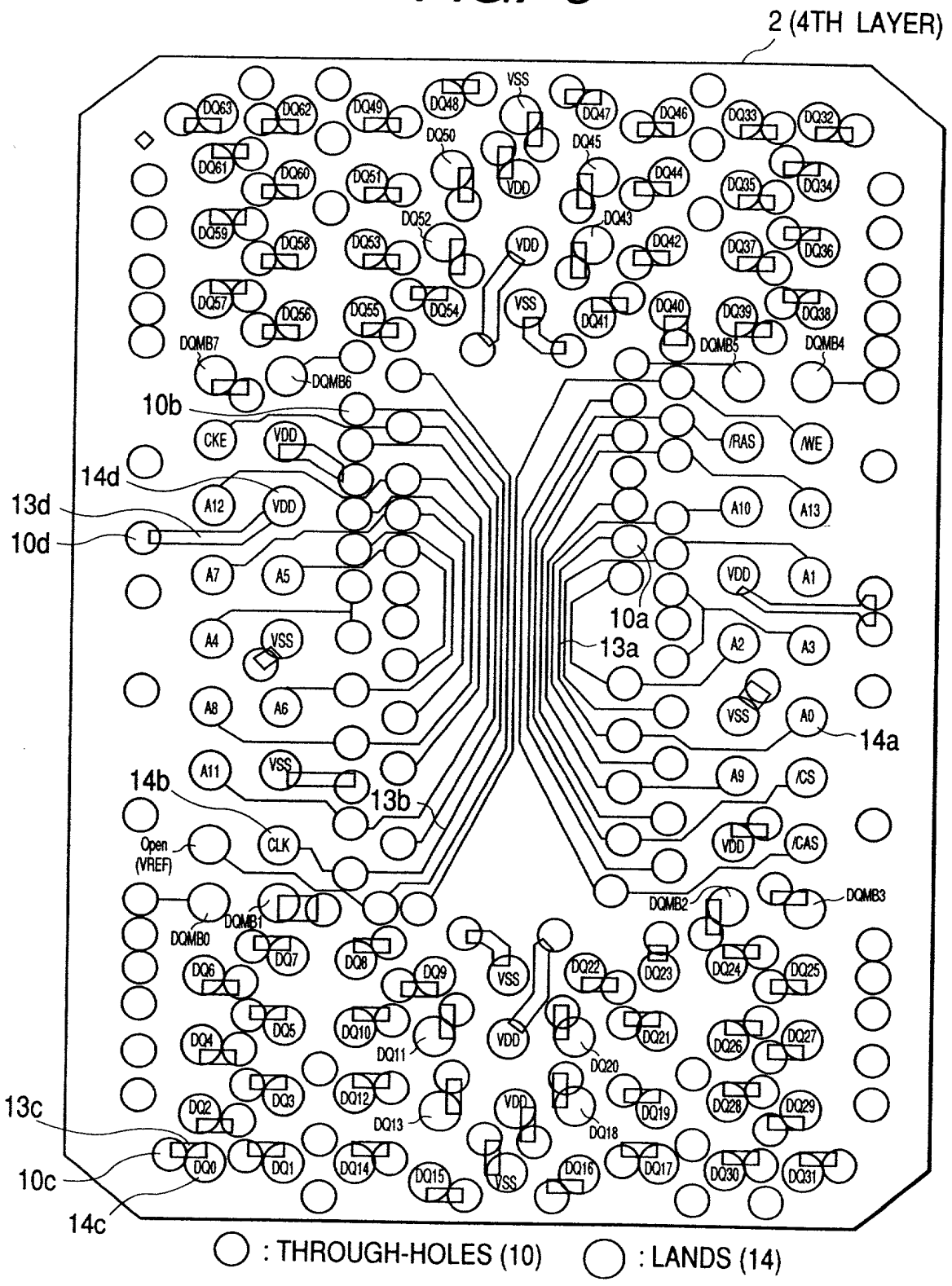

2 (4TH LAYER)
VSS
DQ63
DQ62
DQ49
DQ48
DQ47
DQ46
DQ33
DQ32
DQ50
DQ45
DQ61
DQ60
DQ51
VDD
DQ44
DQ35
DQ34
DQ52
DQ43
DQ59
DQ58
DQ53
VDD
DQ42
DQ37
DQ36
DQ57
DQ56
DQ55
DQ54
VSS
DQ41
DQ40
DQ39
DQ38
DQMB7
DQMB6
DQMB5
DQMB4
10b
CKE
VDD
/RAS
/WE
14d
13d
A12
VDD
A10
A13
10d
A7
A5
VDD
A1
10a
A4
VSS
13a
A2
A3
A8
A6
VSS
A0
14a
A11
VSS
A9
/CS
14b
13b
Open
(VREF)
CLK
VDD
/CAS
DQMB2
DQMB3
DQMB1
DQMB0
DQ7
DQ8
DQ9
VSS
DQ22
DQ23
DQ24
DQ25
DQ6
DQ5
DQ10
DQ11
VDD
DQ21
DQ26
DQ27
DQ4
DQ20
13c
DQ3
DQ12
DQ19
DQ28
DQ29
DQ2
DQ13
VDD
DQ18
DQ0
DQ1
DQ14
DQ15
VSS
DQ16
DQ17
DQ30
DQ31
10c
14c
: THROUGH-HOLES (10)
: LANDS (14)

FIG. 10

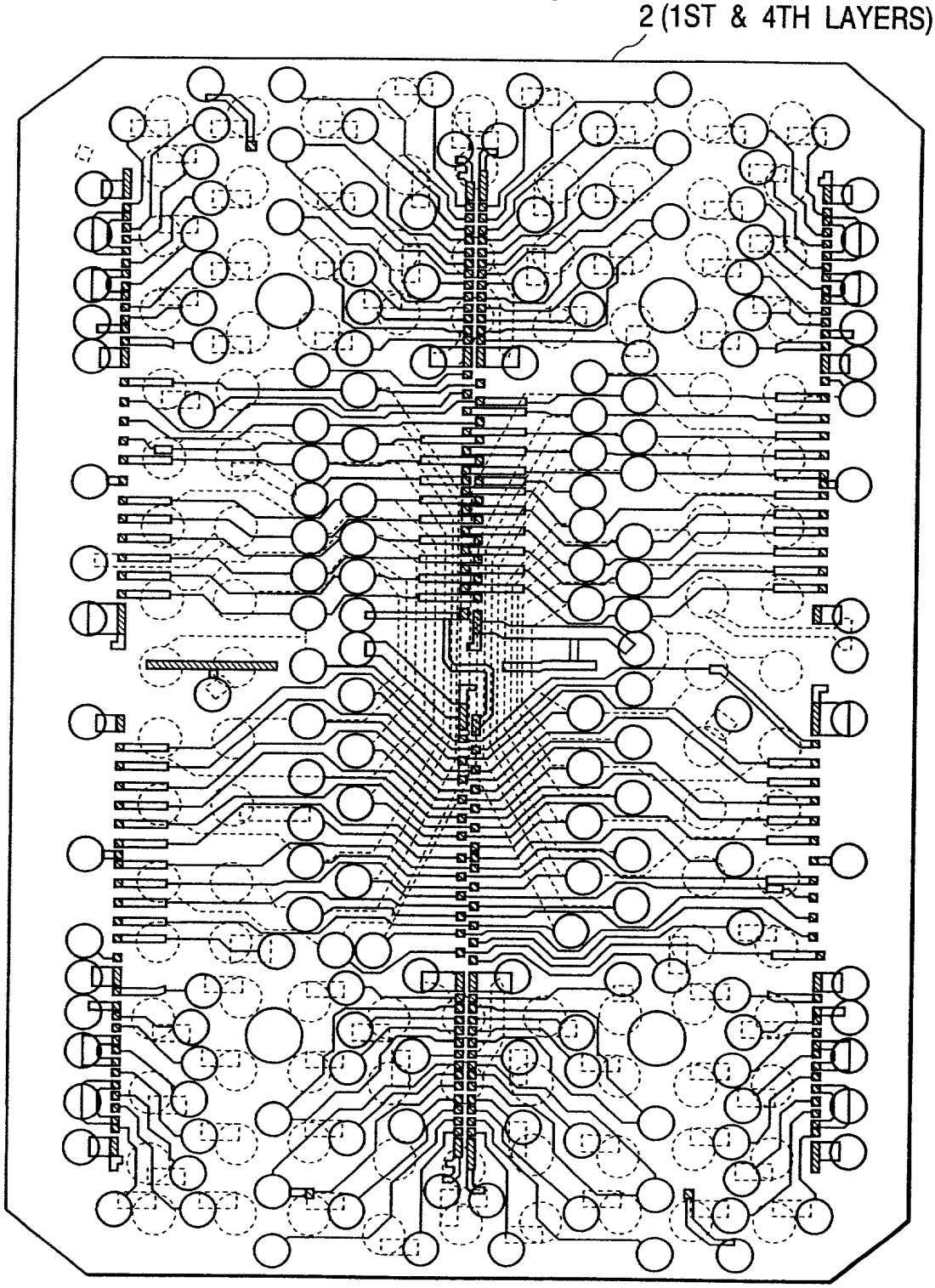


FIG. 11

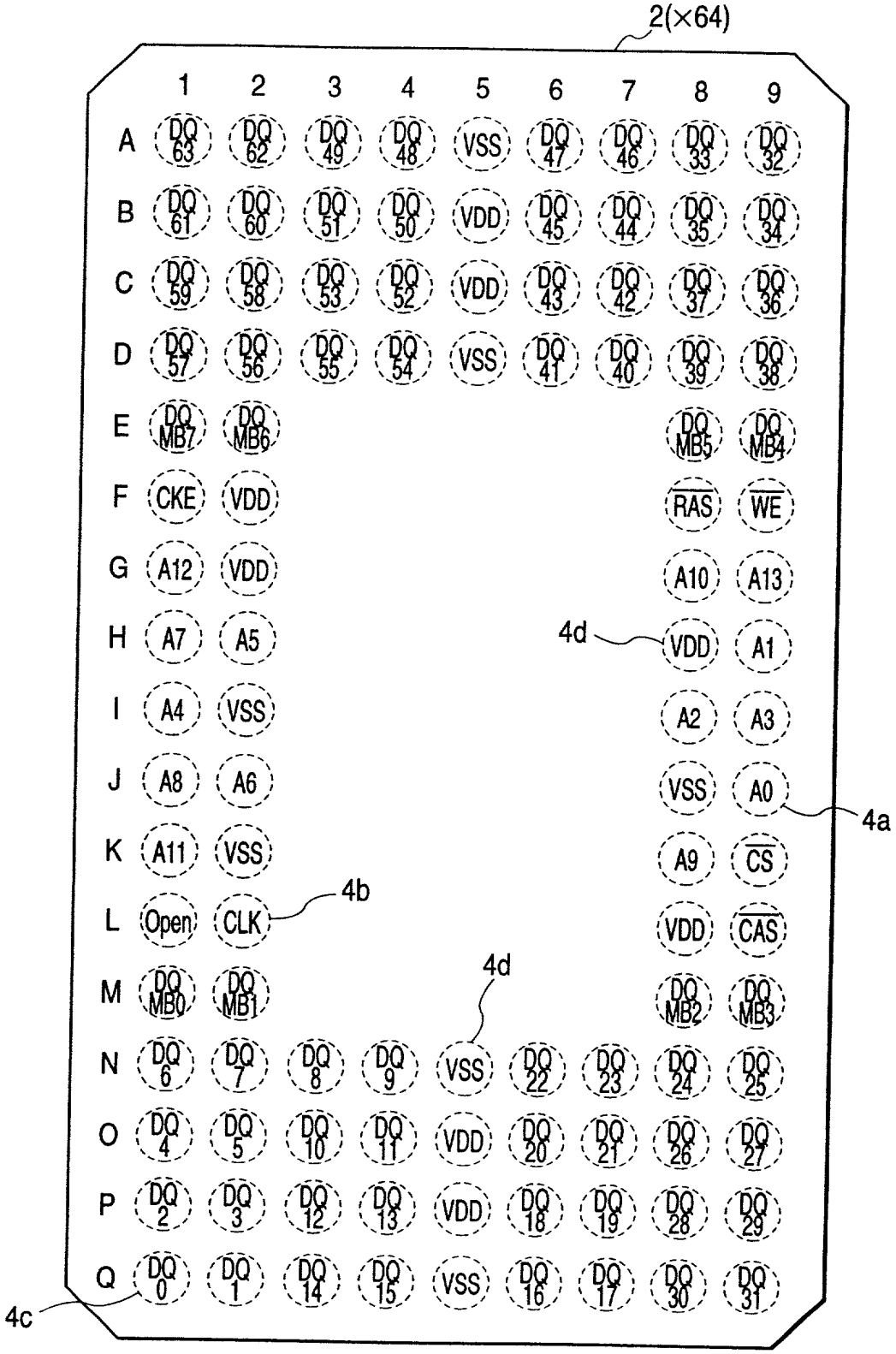

2(×64)
1 2 3 4 5 6 7 8 9
A DQ63 DQ62 DQ49 DQ48 VSS DQ47 DQ46 DQ33 DQ32
B DQ61 DQ60 DQ51 DQ50 VDD DQ45 DQ44 DQ35 DQ34
C DQ59 DQ58 DQ53 DQ52 VDD DQ43 DQ42 DQ37 DQ36
D DQ57 DQ56 DQ55 DQ54 VSS DQ41 DQ40 DQ39 DQ38
E DQMB7 DQMB6 DQMB5 DQMB4
F CKE VDD RAS WE
G A12 VDD A10 A13
H A7 A5 VDD A1
I A4 VSS A2 A3
J A8 A6 VSS A0
K A11 VSS A9 CS
L Open CLK VDD CAS
M DQMB0 DQMB1 DQMB2 DQMB3
N DQ6 DQ7 DQ8 DQ9 VSS DQ22 DQ23 DQ24 DQ25
O DQ4 DQ5 DQ10 DQ11 VDD DQ20 DQ21 DQ26 DQ27
P DQ2 DQ3 DQ12 DQ13 VDD DQ18 DQ19 DQ28 DQ29
Q DQ0 DQ1 DQ14 DQ15 VSS DQ16 DQ17 DQ30 DQ31
4a
4b
4c
4d
4d

FIG. 12

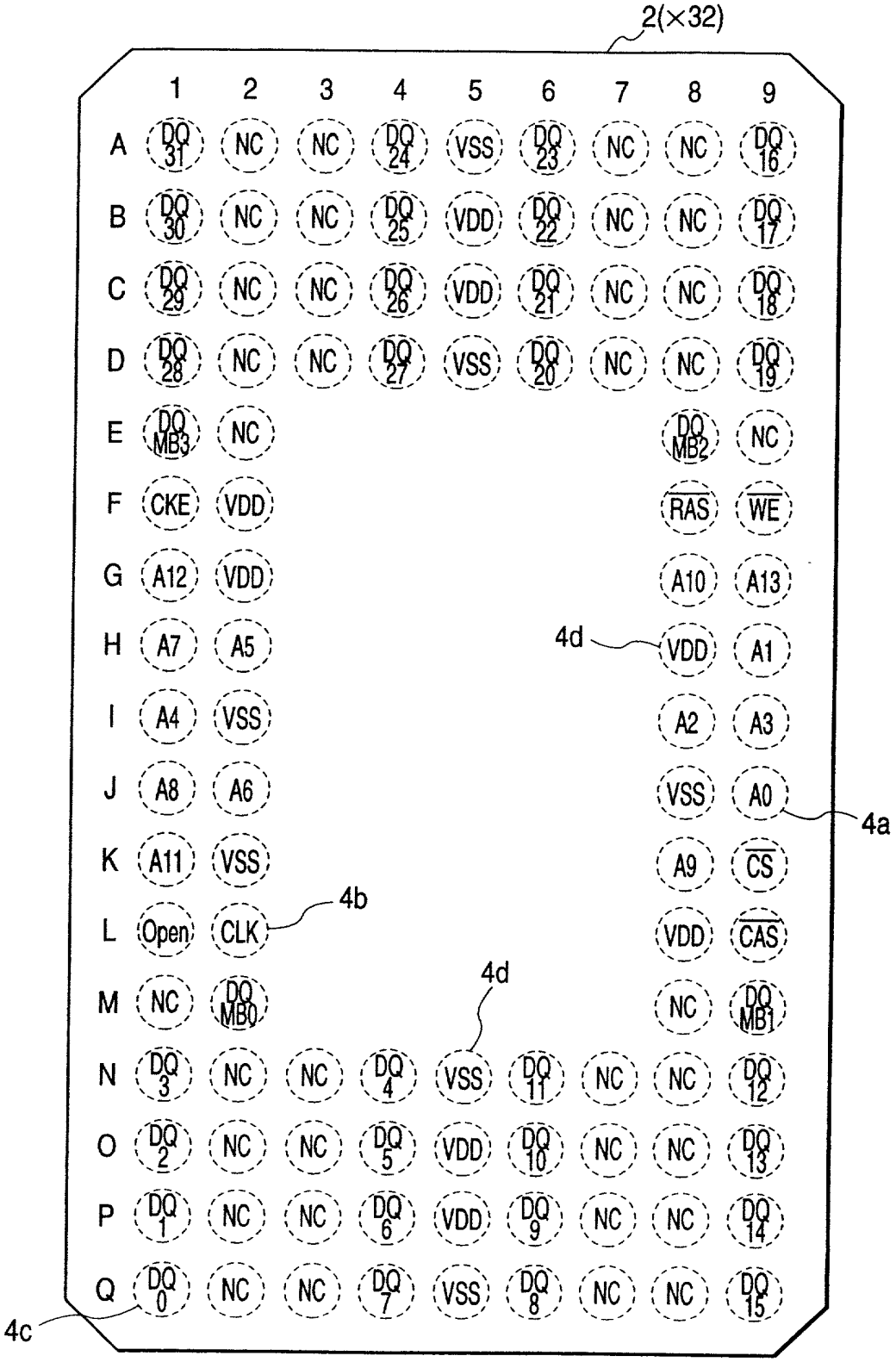

2(×32)
1 2 3 4 5 6 7 8 9
A DQ31 NC NC DQ24 VSS DQ23 NC NC DQ16
B DQ30 NC NC DQ25 VDD DQ22 NC NC DQ17
C DQ29 NC NC DQ26 VDD DQ21 NC NC DQ18
D DQ28 NC NC DQ27 VSS DQ20 NC NC DQ19
E DQMB3 NC DQMB2 NC
F CKE VDD RAS WE
G A12 VDD A10 A13
H A7 A5 VDD A1
I A4 VSS A2 A3
J A8 A6 VSS A0
K A11 VSS A9 CS
L Open CLK VDD CAS
M NC DQMB0 NC DQMB1
N DQ3 NC NC DQ4 VSS DQ11 NC NC DQ12
O DQ2 NC NC DQ5 VDD DQ10 NC NC DQ13
P DQ1 NC NC DQ6 VDD DQ9 NC NC DQ14
Q DQ0 NC NC DQ7 VSS DQ8 NC NC DQ15
4a
4b
4c
4d
4d

FIG. 13

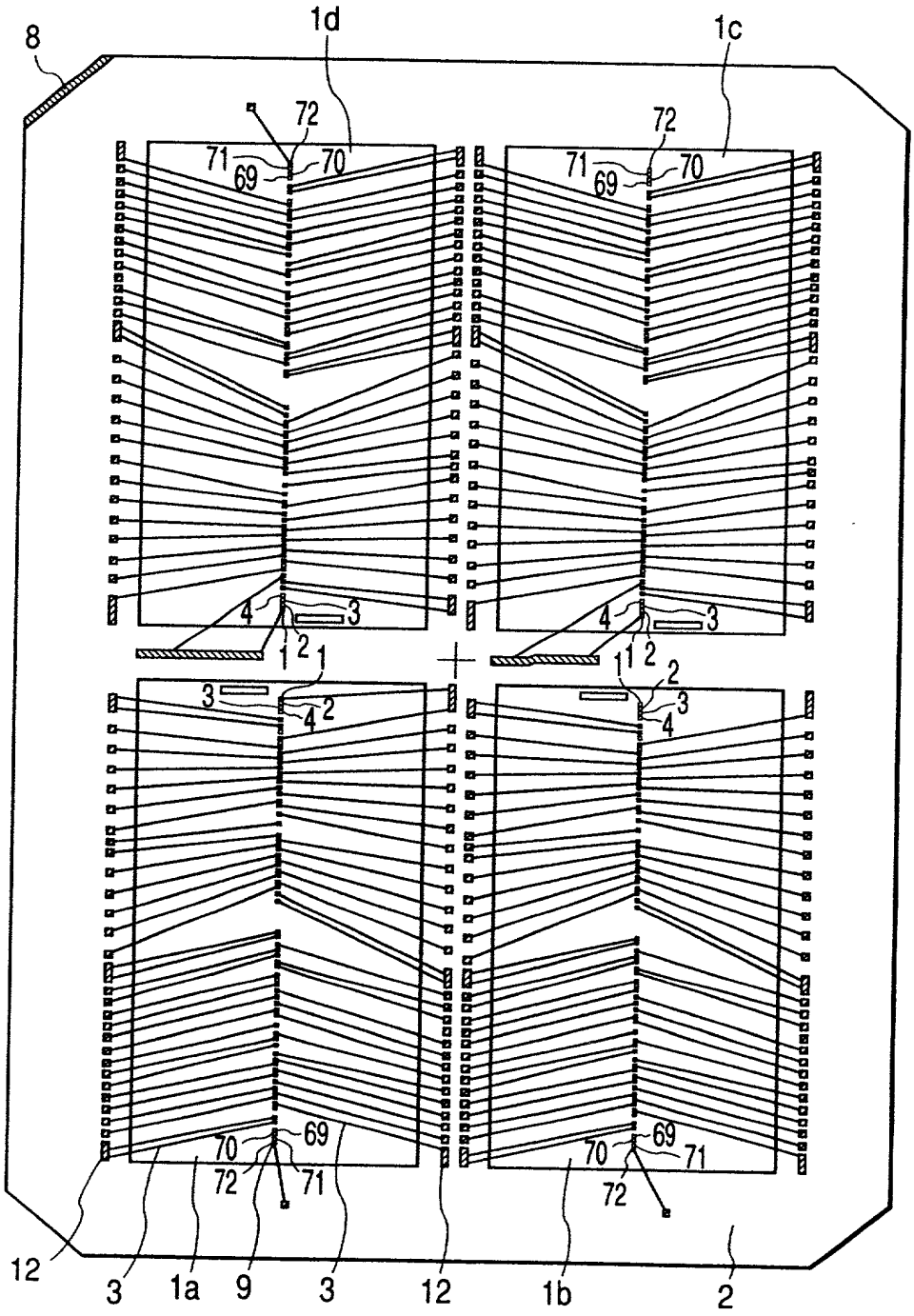
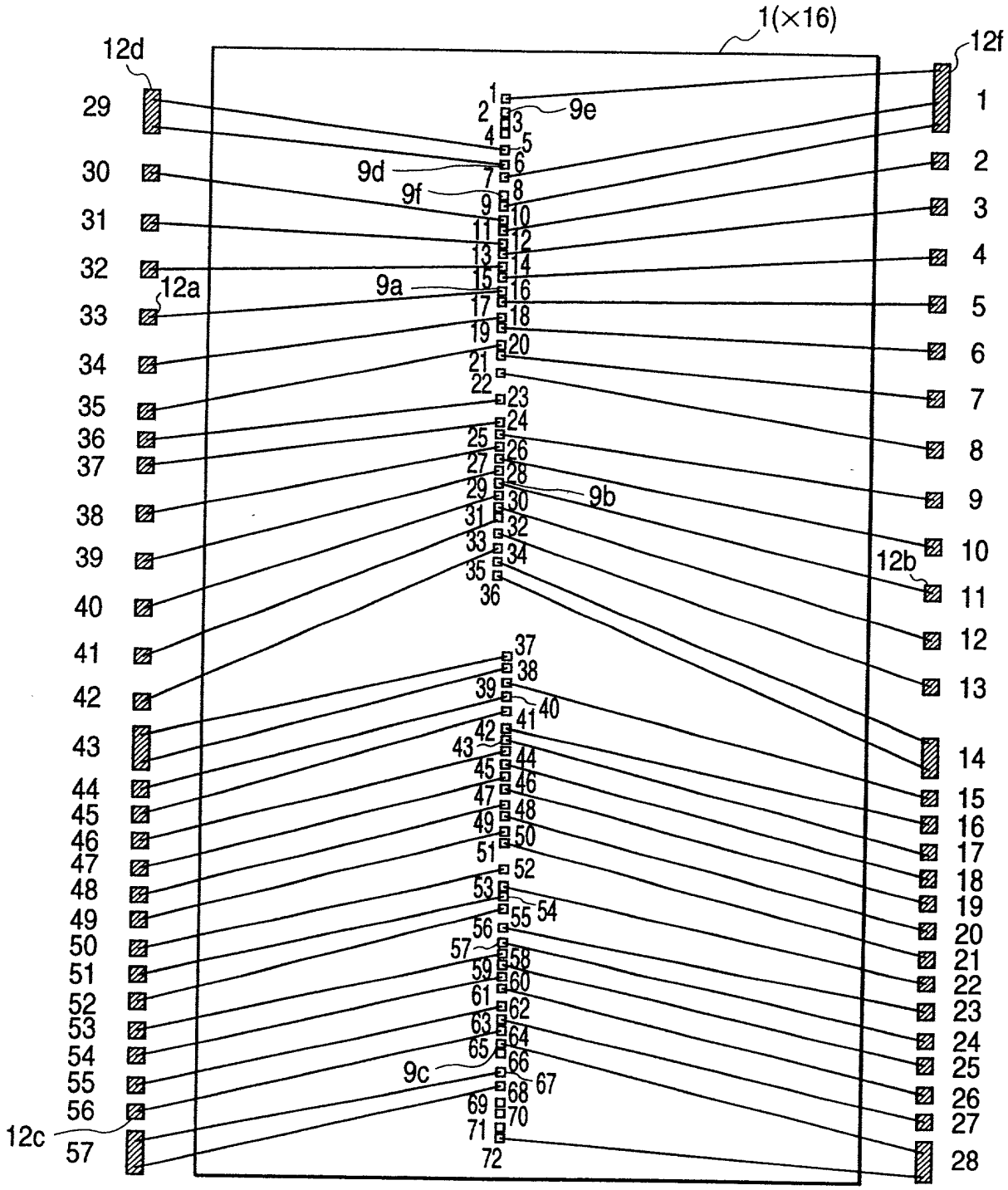


FIG. 14


1(×16)
12d
12f
12a
12b
12c
9a
9b
9c
9d
9e
9f
29
30
31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
53
54
55
56
57
1
2
3
4
5
6
7
8
9
10
11
12
13
14
15
16
17
18
19
20
21
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23
24
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27
28
29
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31
32
33
34
35
36
37
38
39
40
41
42
43
44
45
46
47
48
49
50
51
52
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71
72

FIG. 15

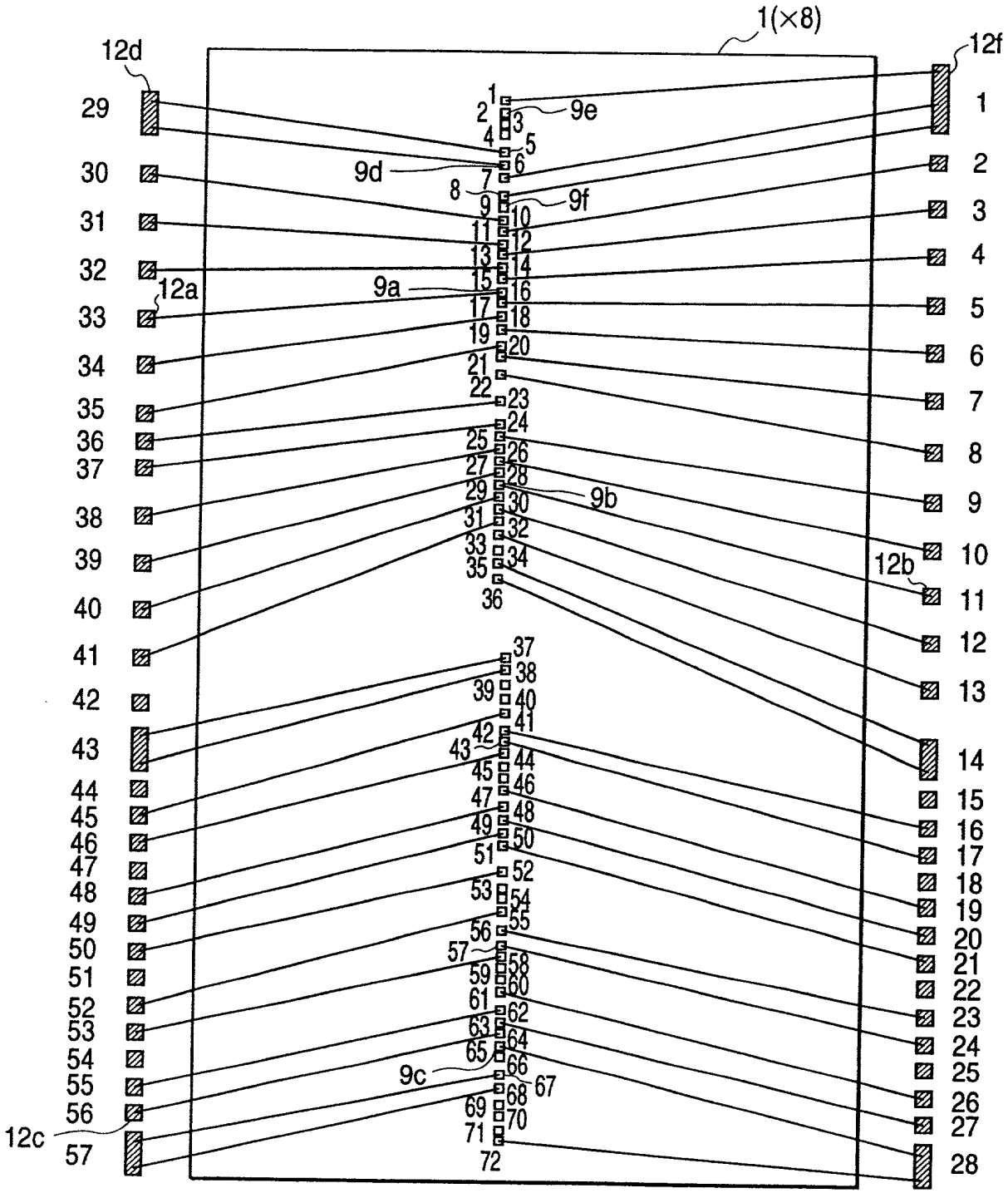

FIG. 16

PAD NO.	PAD NAMES	USE
1	VSSI	POWER SUPPLY
2	VBB	P-TEST
3	VPLT	P-TEST
4	VPP	P-TEST
5	VDDI	POWER SUPPLY
6	VDD	POWER SUPPLY
7	VSS	POWER SUPPLY
8	BOP1B	BONDING OPTION
9	BOP2B	BONDING OPTION
10	A3	INPUT (ADDRESS)
11	A4	INPUT (ADDRESS)
12	A2	INPUT (ADDRESS)
13	A5	INPUT (ADDRESS)
14	A1	INPUT (ADDRESS)
15	A6	INPUT (ADDRESS)
16	A0	INPUT (ADDRESS)
17	A7	INPUT (ADDRESS)
18	A10	INPUT (ADDRESS)
19	A8	INPUT (ADDRESS)
20	A12	INPUT (ADDRESS)
21	A9	INPUT (ADDRESS)
22	VSS	POWER SUPPLY
23	VDD	POWER SUPPLY
24	A13	INPUT (ADDRESS)
25	A11	INPUT (ADDRESS)
26	/CS	INPUT (CONTROL)
27	CKE	INPUT (CONTROL)
28	/RAS	INPUT (CONTROL)
29	CLK	INPUT (CONTROL)
30	/CAS	INPUT (CONTROL)
31	DQMU	INPUT (CONTROL)
32	/WE	INPUT (CONTROL)
33	VREF	INPUT (CONTROL)
34	DQML	INPUT (CONTROL)
35	VSSI	POWER SUPPLY
36	VSS	POWER SUPPLY
	CHIP CENTER	

PAD NO.	PAD NAMES	USE
37	VDD	POWER SUPPLY
38	VDDI	POWER SUPPLY
39	DQ8	I/O DATA
40	DQ7	I/O DATA
41	VDDQ	POWER SUPPLY
42	VSSQ	POWER SUPPLY
43	DQ9	I/O DATA
44	DQ6	I/O DATA
45	DQ10	I/O DATA
46	DQ5	I/O DATA
47	VSSQ	POWER SUPPLY
48	VDDQ	POWER SUPPLY
49	DQ11	I/O DATA
50	DQ4	I/O DATA
51	VSS	POWER SUPPLY
52	VDD	POWER SUPPLY
53	DQ12	I/O DATA
54	DQ3	I/O DATA
55	VDDQ	POWER SUPPLY
56	VSSQ	POWER SUPPLY
57	DQ13	I/O DATA
58	DQ2	I/O DATA
59	DQ14	I/O DATA
60	DQ1	I/O DATA
61	VSSQ	POWER SUPPLY
62	VDDQ	POWER SUPPLY
63	DQ15	I/O DATA
64	DQ0	I/O DATA
65	VSS	POWER SUPPLY
66	BOP0B	BONDING OPTION
67	VDD	POWER SUPPLY
68	VDDIU	POWER SUPPLY
69	VPERI	P-TEST
70	VDL	P-TEST
71	VBLR	P-TEST
72	VSSIU	POWER SUPPLY
	CHIP CENTER	

FIG. 17

SUBSTRATE PAD NO.	CHIP PAD NAMES ×16	CHIP PAD NAMES ×8
1	VSS	VSS
	VSS	VSS
	BOP2B	—
	—	BOP1B
2	A4	A4
3	A5	A5
4	A6	A6
5	A7	A7
6	A8	A8
7	A12	A12
8	VSS	VSS
9	A11	A11
10	CKE	CKE
11	CLK	CLK
12	/WE	/WE
13	VREF	VREF
14	VSS	VSS
	VSS	VSS
15	DQ8	—
16	VSS	VSS
17	DQ9	DQ4
18	DQ10	—
19	VSS	VSS
20	DQ11	DQ5
21	VSS	VSS
22	DQ12	—
23	VSS	VSS
24	DQ13	DQ6
25	DQ14	—
26	VSS	VSS
27	DQ15	DQ7
28	VSS	VSS
	VSS	VSS

SUBSTRATE PAD NO.	CHIP PAD NAMES ×16	CHIP PAD NAMES ×8
29	VDD	VDD
	VDD	VDD
30	A3	A3
31	A2	A2
32	A1	A1
33	A0	A0
34	A10	A10
35	A9	A9
36	VDD	VDD
37	A13	A13
38	/CS	/CS
39	/RAS	/RAS
40	/CAS	/CAS
41	DQMU	DQM
42	DQML	—
43	VDD	VDD
	VDD	VDD
44	DQ7	—
45	VDD	VDD
46	DQ6	DQ3
47	DQ5	—
48	VDD	VDD
49	DQ4	DQ2
50	VDD	VDD
51	DQ3	—
52	VDD	VDD
53	DQ2	DQ1
54	DQ1	—
55	VDD	VDD
56	DQ0	DQ0
57	VDD	VDD
	VDD	VDD

— : NC

FIG. 18

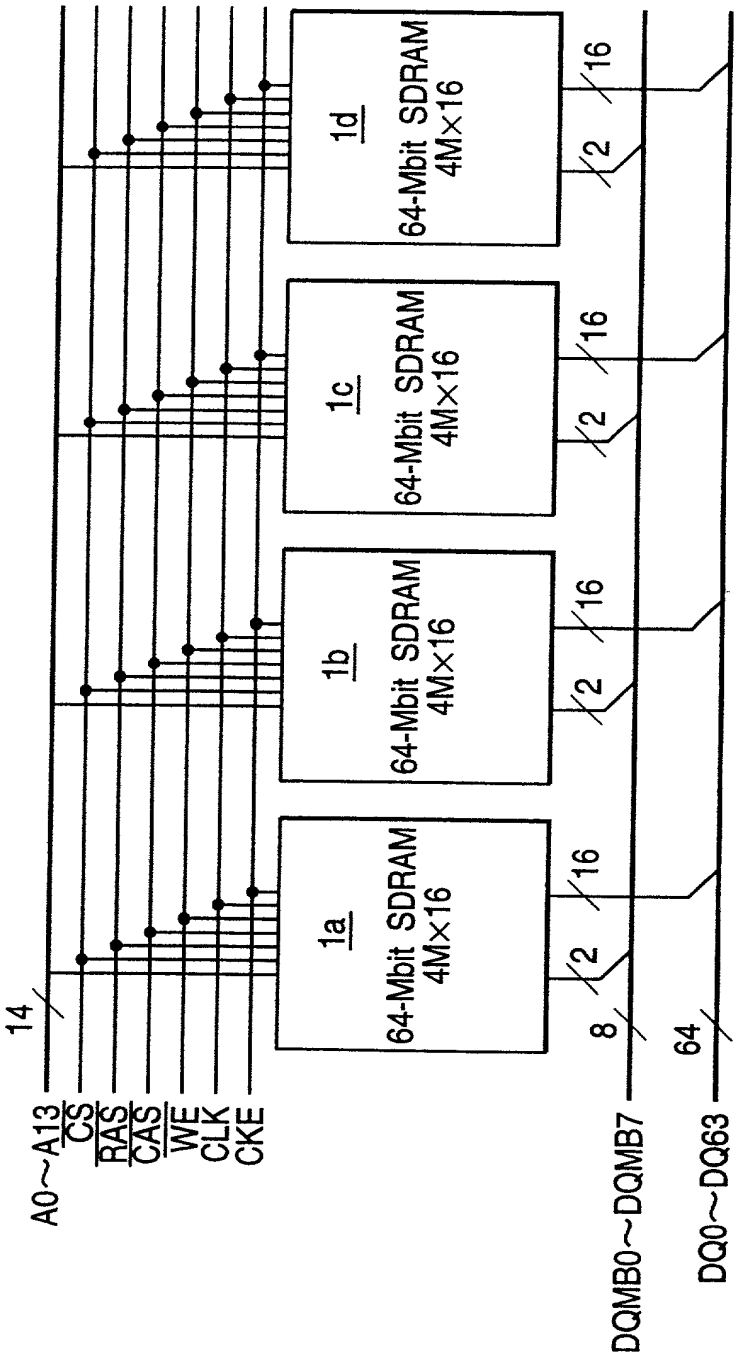
1a
64-Mbit SDRAM
4M×16
1b
64-Mbit SDRAM
4M×16
1c
64-Mbit SDRAM
4M×16
1d
64-Mbit SDRAM
4M×16
14
A0~A13
CS
RAS
CAS
WE
CLK
CKE
2
16
8
64
DQMB0~DQMB7
DQ0~DQ63

FIG. 19

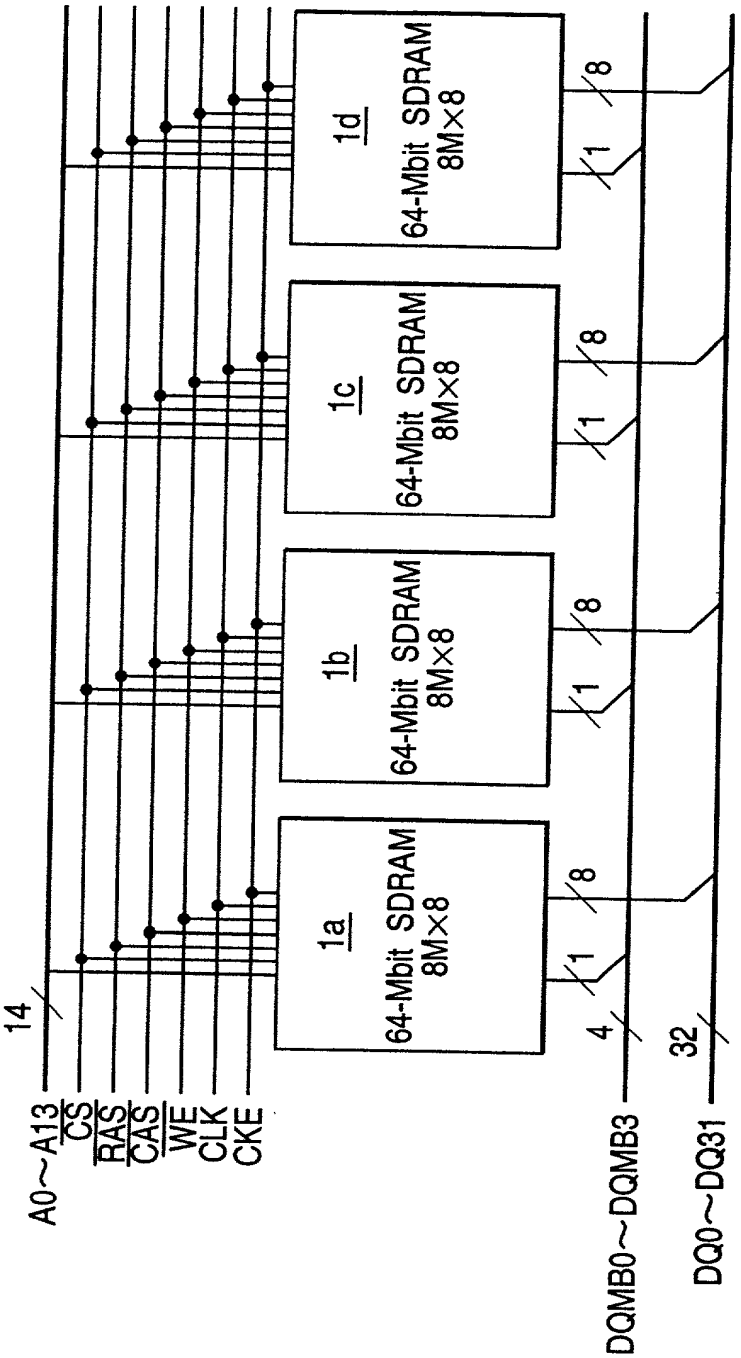
14
A0~A13
CS
RAS
CAS
WE
CLK
CKE
1a
64-Mbit SDRAM
8M×8
1b
64-Mbit SDRAM
8M×8
1c
64-Mbit SDRAM
8M×8
1d
64-Mbit SDRAM
8M×8
1
8
4
32
DQMB0~DQMB3
DQ0~DQ31

FIG. 20

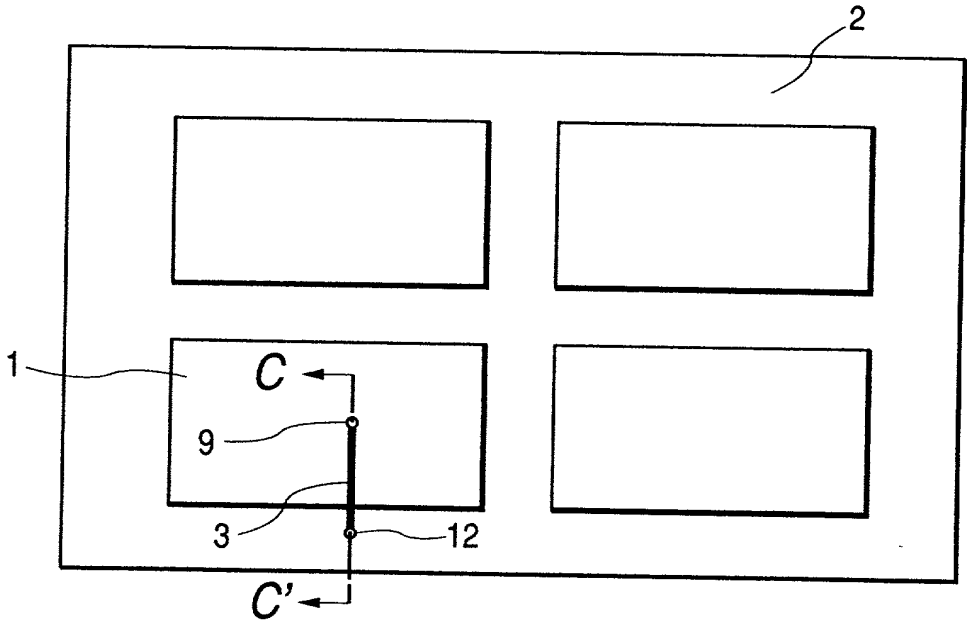

FIG. 21

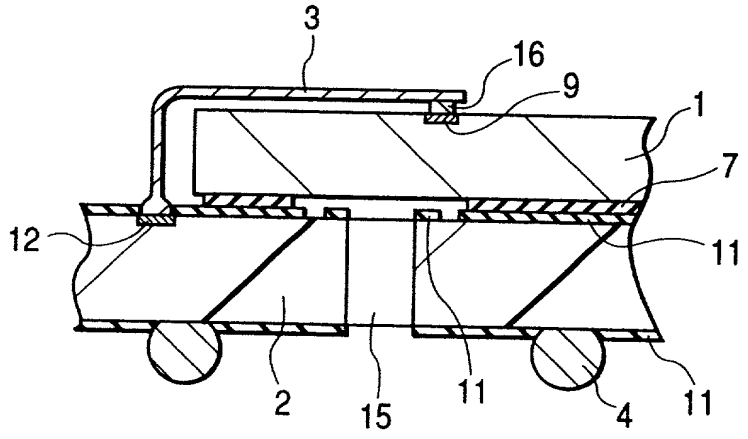

FIG. 22

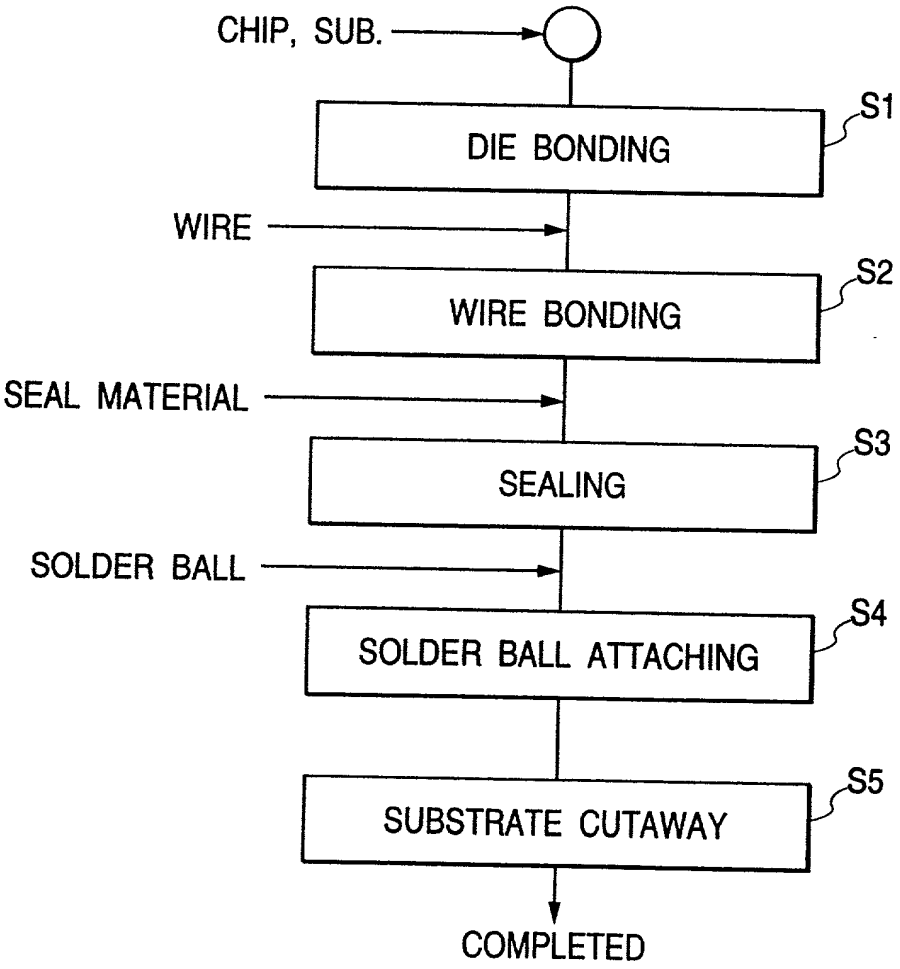
CHIP, SUB.
DIE BONDING
S1
WIRE
WIRE BONDING
S2
SEAL MATERIAL
SEALING
S3
SOLDER BALL
SOLDER BALL ATTACHING
S4
SUBSTRATE CUTAWAY
S5
COMPLETED

FIG. 23

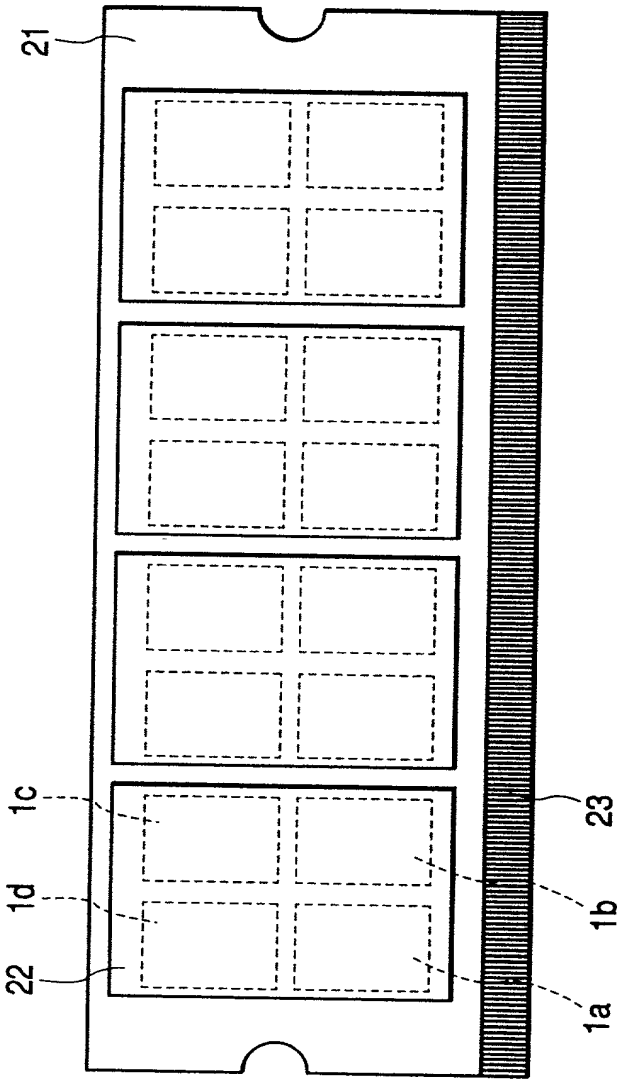

FIG. 24

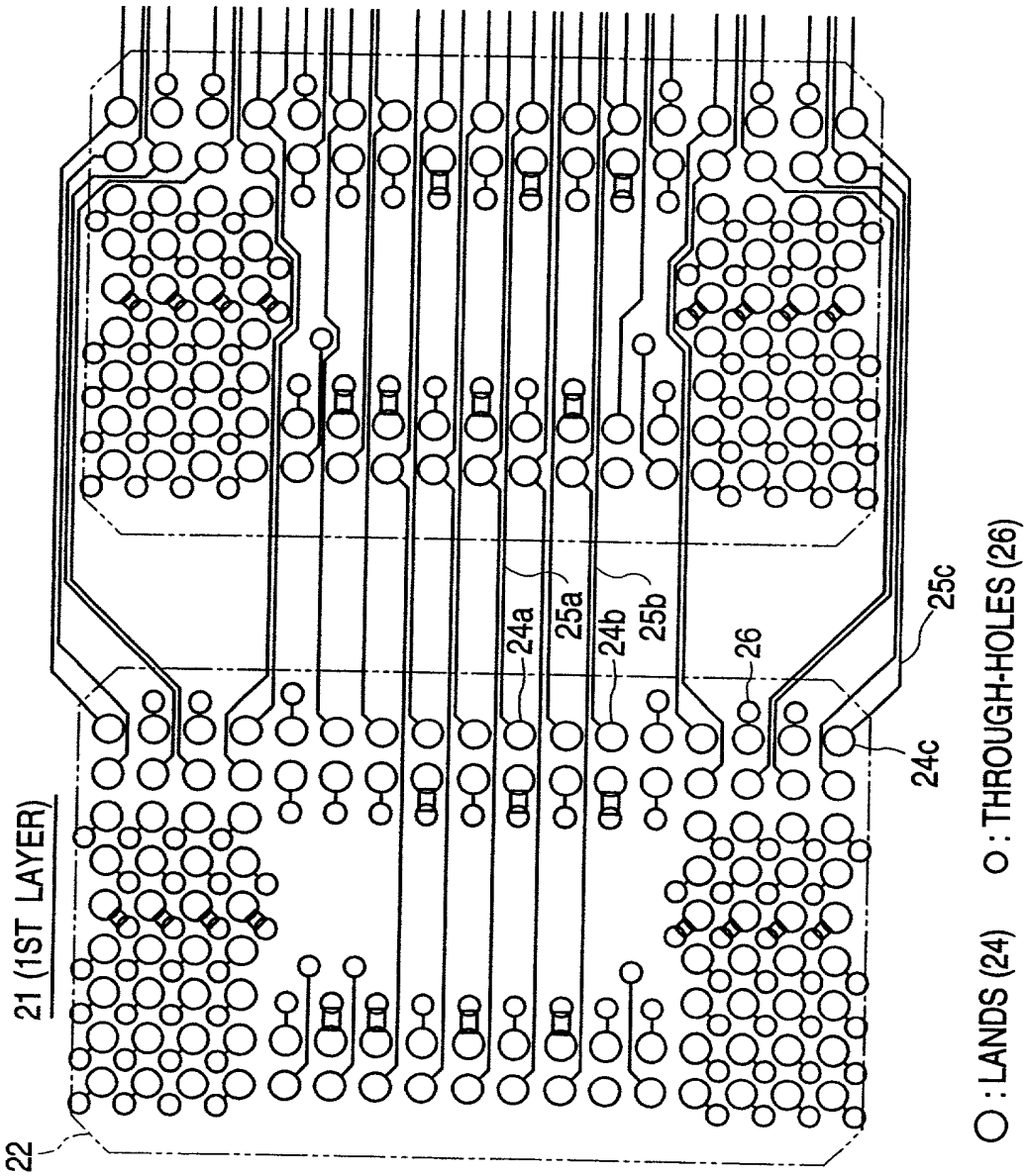
21 (1ST LAYER)
22
24a
25a
24b
25b
26
25c
24c
○ : LANDS (24)
○ : THROUGH-HOLES (26)

FIG. 25

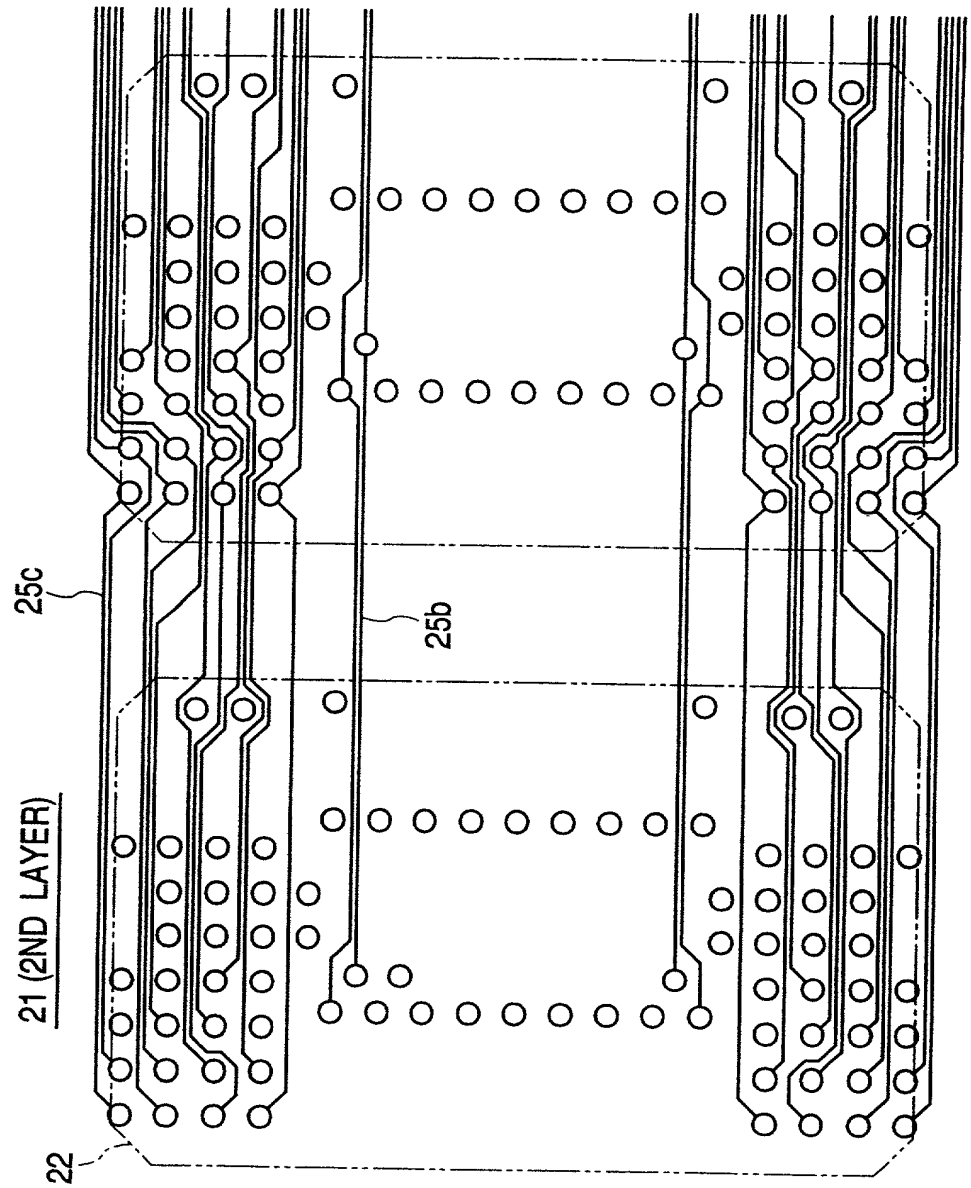

FIG. 26

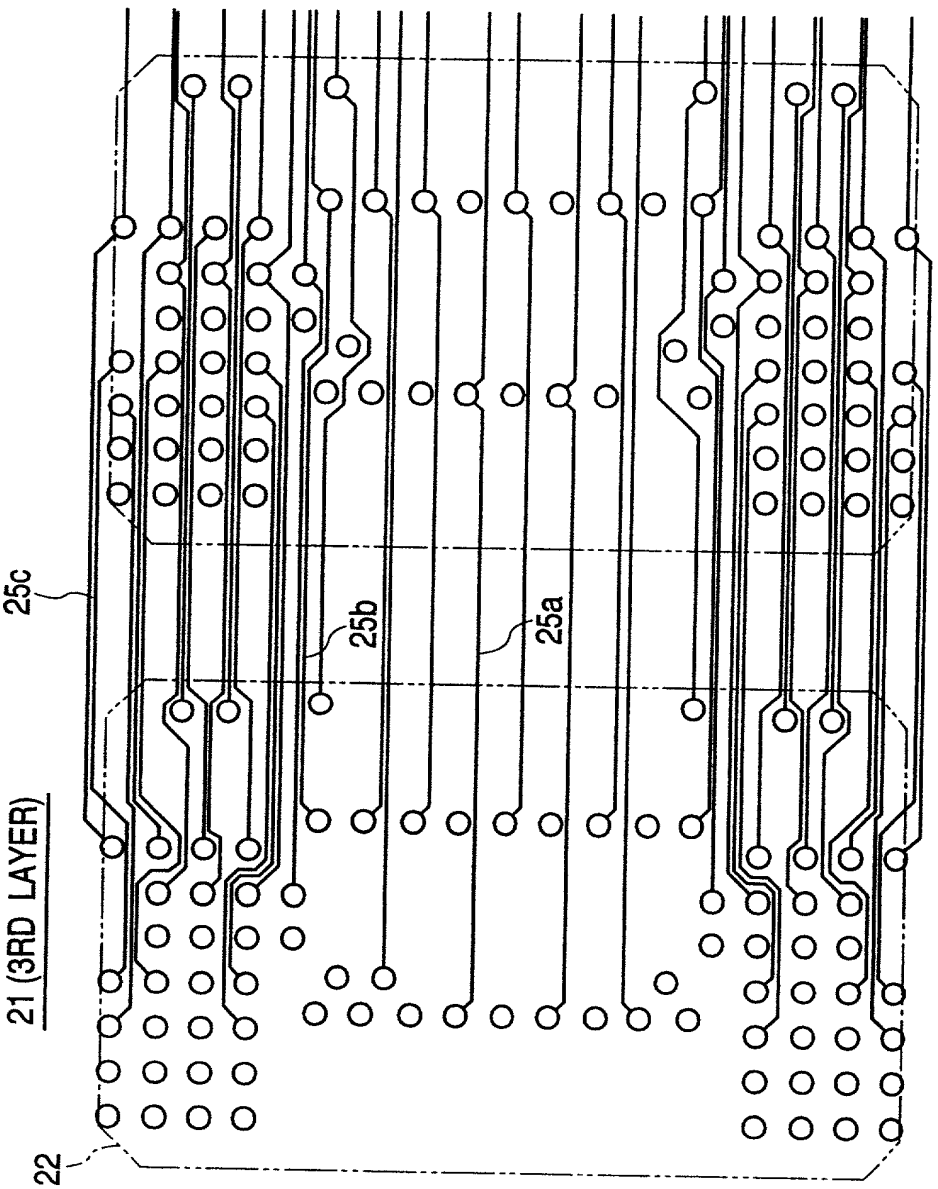

FIG. 27

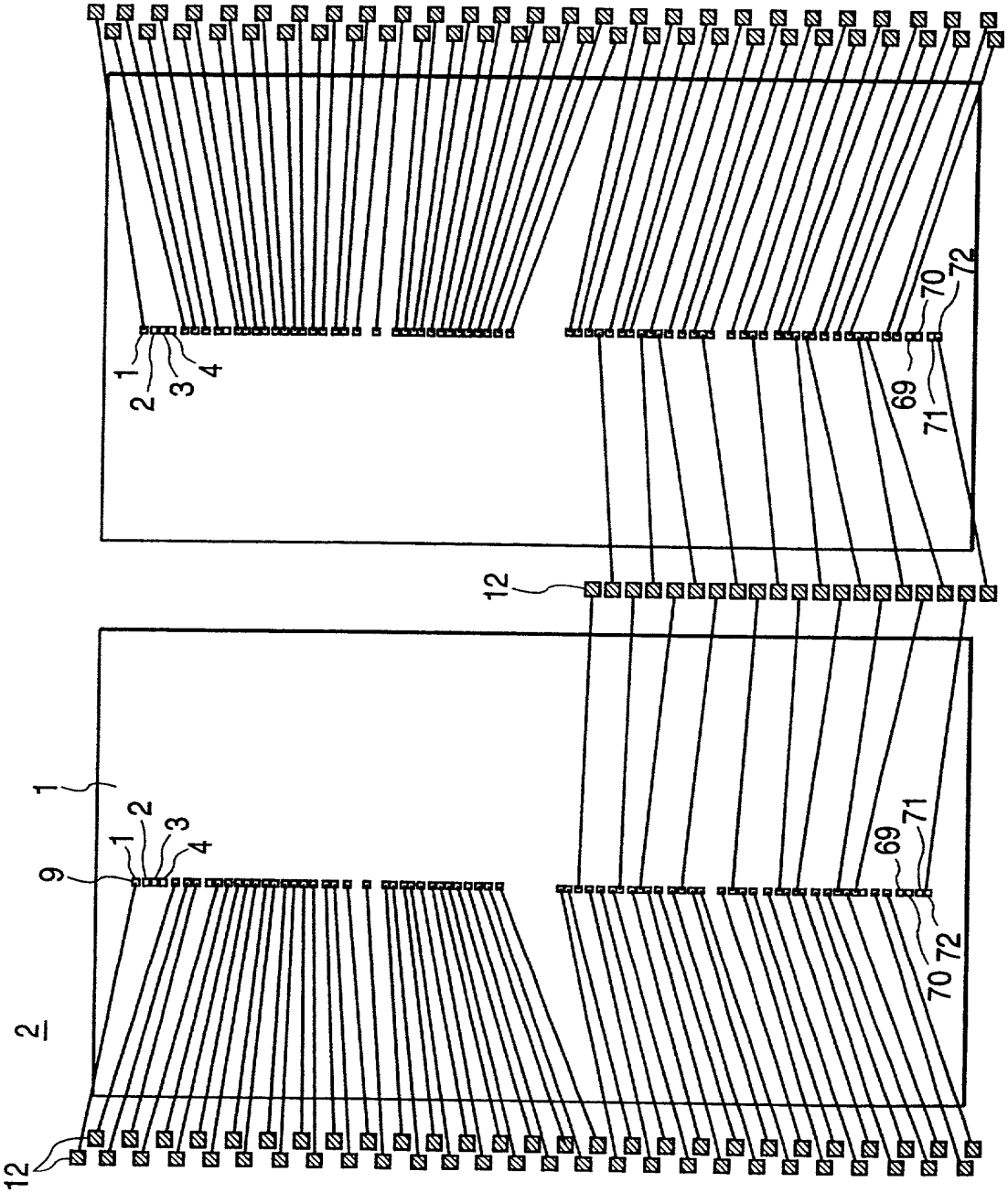

FIG. 28

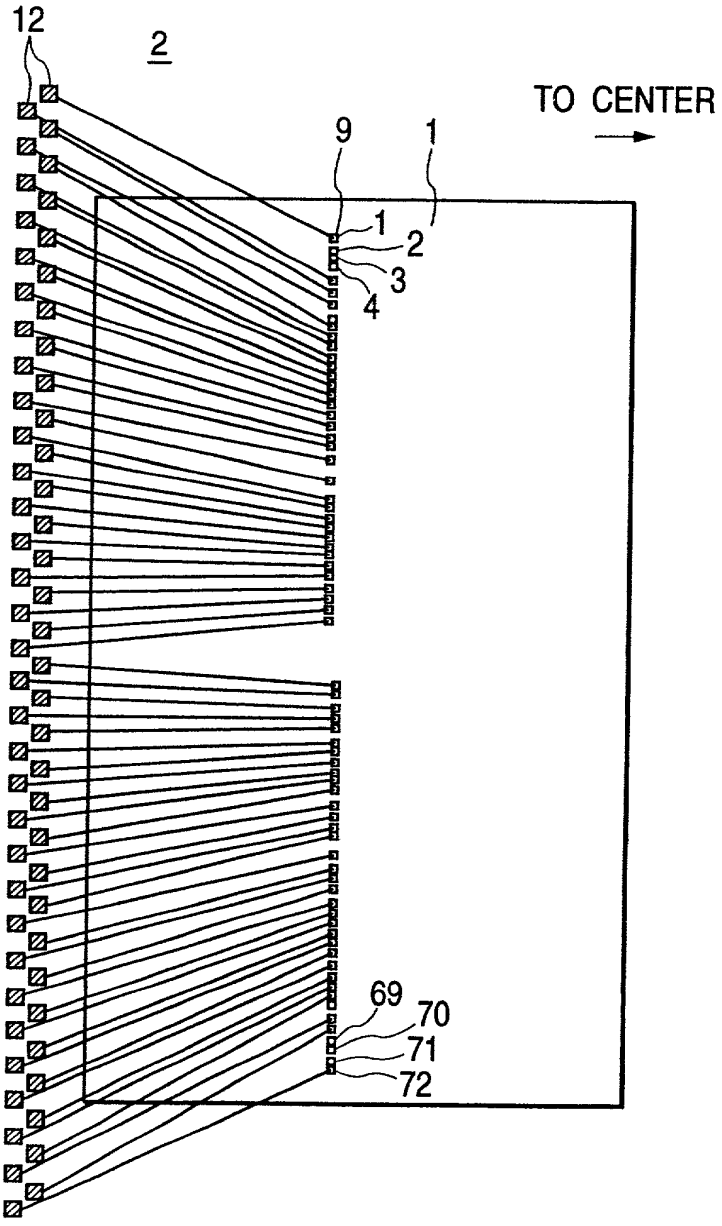

FIG. 29

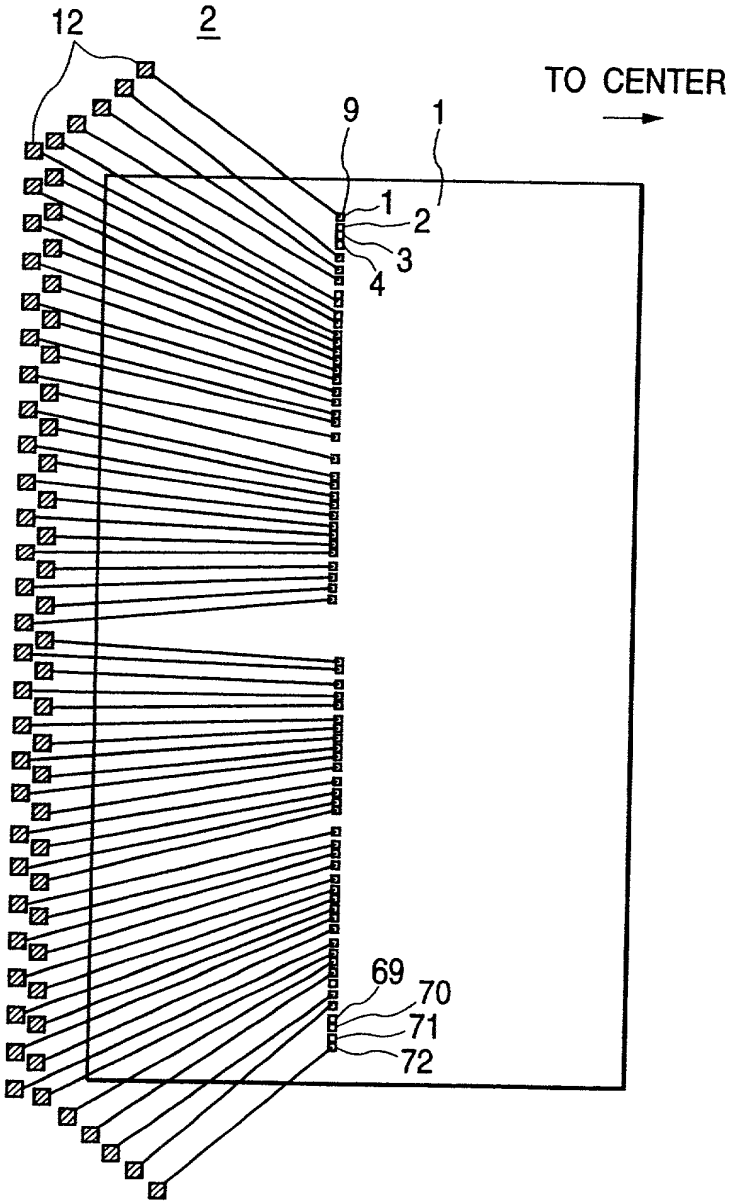

FIG. 30

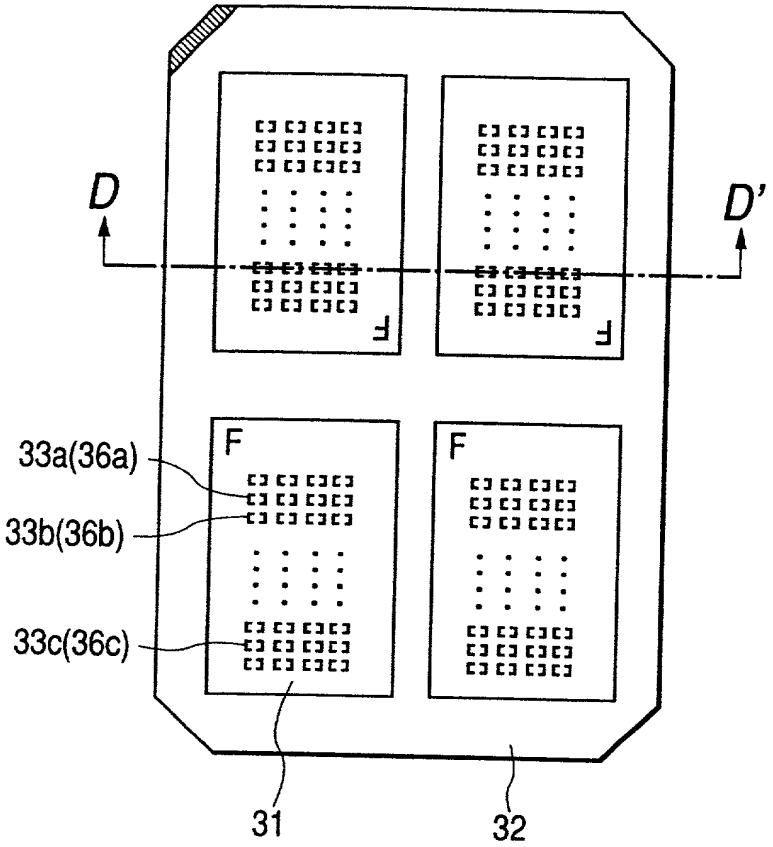

FIG. 31

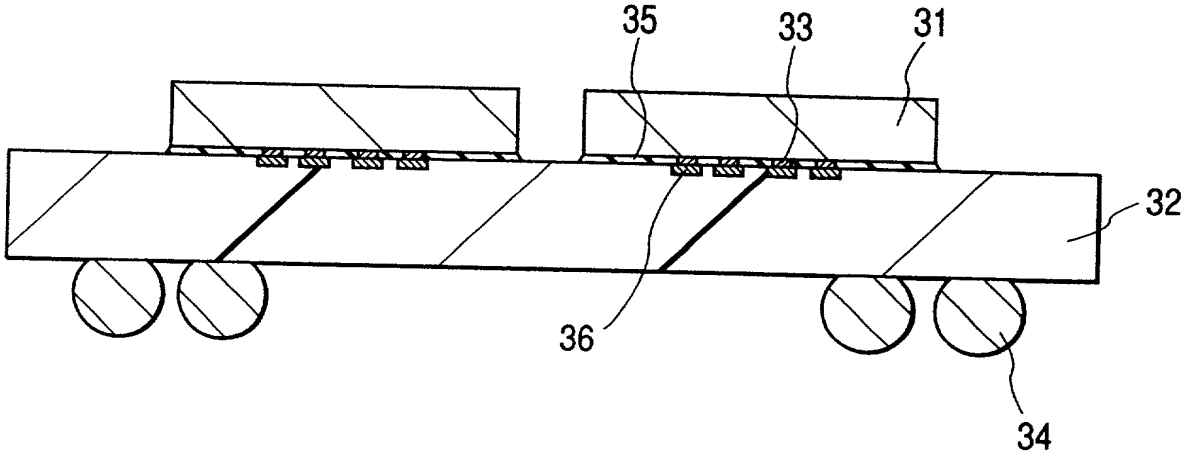

FIG. 32

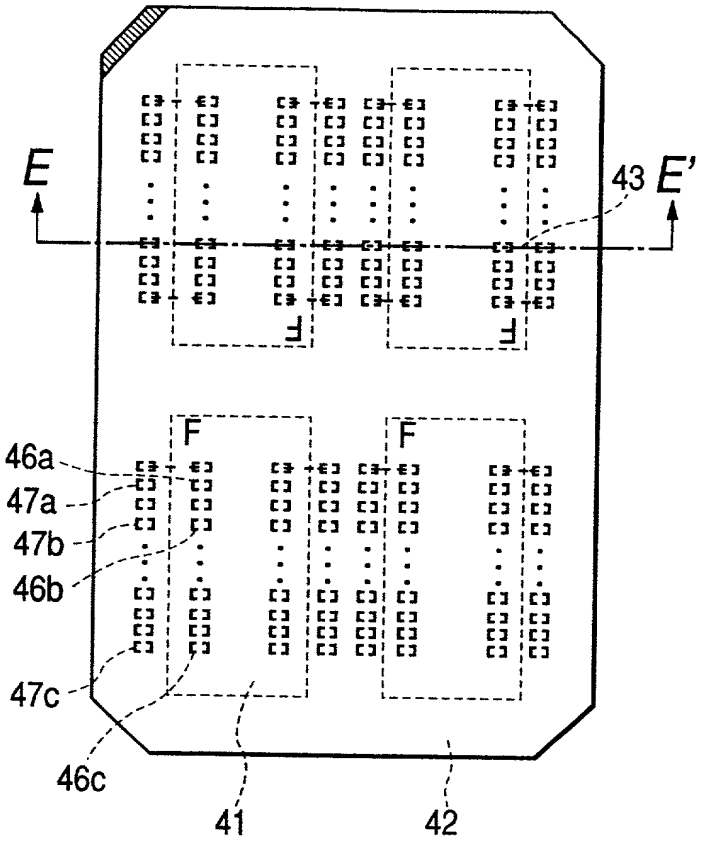

FIG. 33